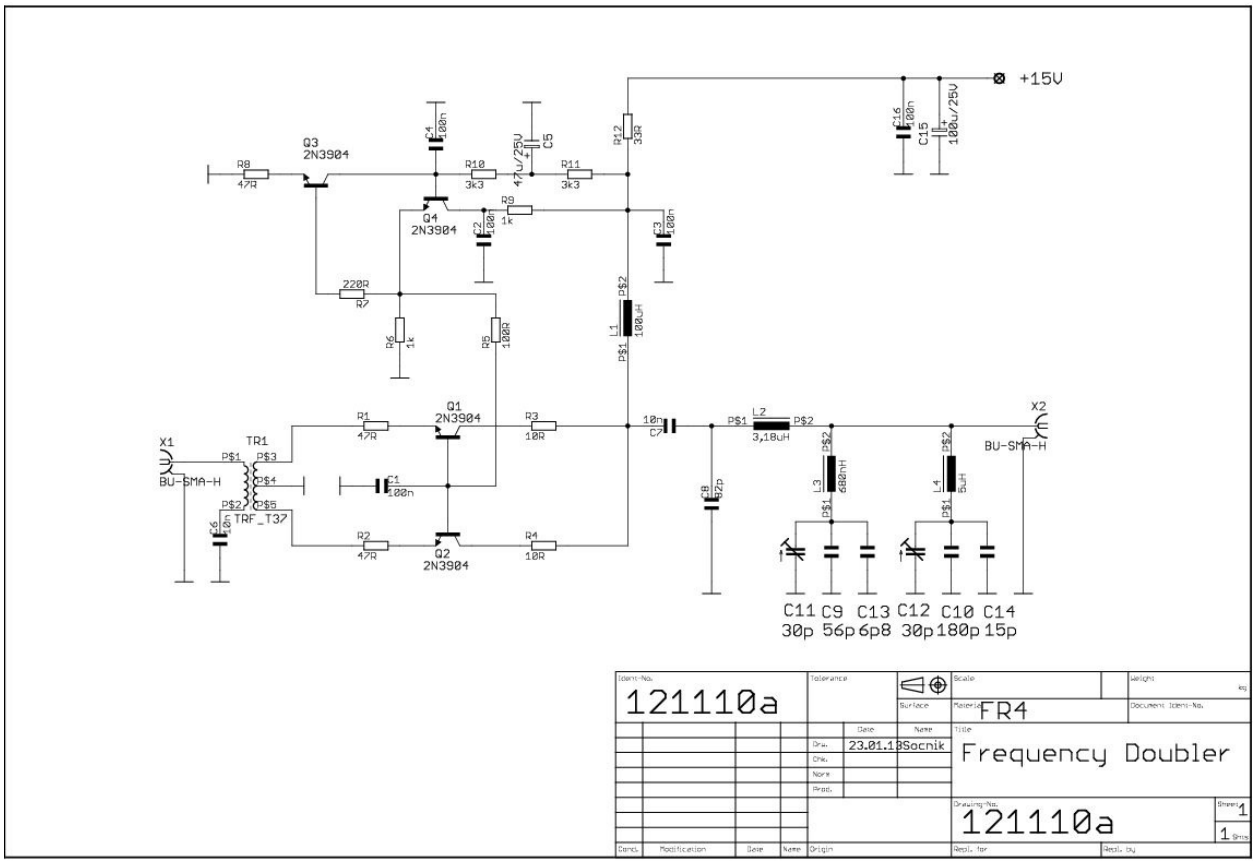
HIGH PERFORMANCE FREQUENCY DOUBLER

For calibration and testing of oscillators by frequency standard laboratories, there is a need to convert 5 MHz signals to the nowadays more common frequency of 10MHz, without affecting the original stability and phase noise characteristics of the 5 MHz input signal.

This paper presents a high performance frequency doubler with excellent short-term stability and ultra-low phase noise as a useful high performance tool for the time and frequency laboratory. The input and output impedance and phase noise of a frequency doubler are not the only important parameters that need to be considered. Other important terms such as the gain, stability over temperature, harmonic distortion, construction techniques, and design practices must be taken into account. Most of these parameters can be rigorously related in an equation to deliver an expected level of performance from the system. Typical manufacturing and design practices that are necessary to ensure a reliable device are presented.

The idea for this circuit which is based on a NIST publication was contributed by Bruce Griffiths when we were discussing the required performance. Several samples have been built in order to improve the output filtering and to characterize the performance extensively.

A differential input two transistor common base configuration with parallel connected collectors was chosen to achieve a power gain of close to one. The output filter matches the transistor output impedance to the 50 Ohm load. It includes traps for the 5 MHz fundamental and 20 MHz harmonic.

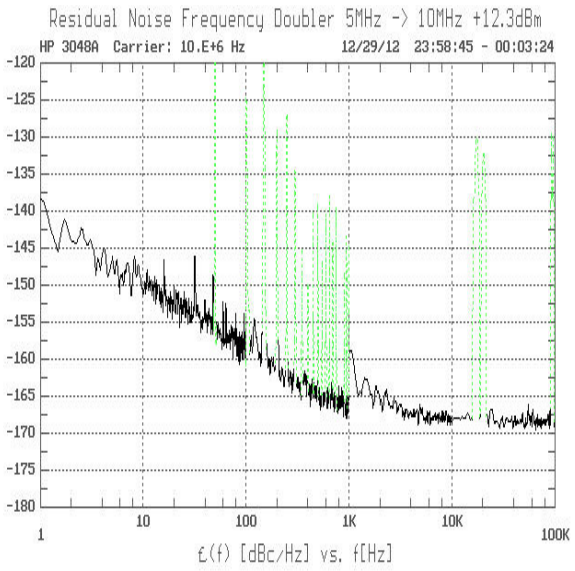


TR1 + L1: FT37 - 43 ferrite toroidal core (example: RS p.n. 467-4093)
L2 + L3 + L4 : T37 - 2 red iron powder toroidal core

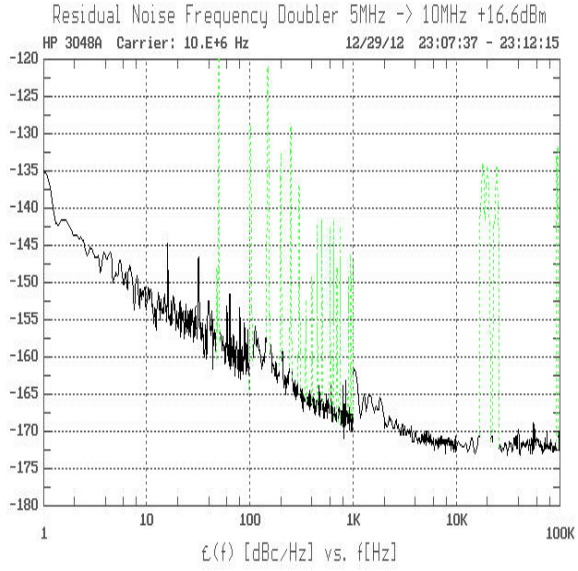
TR1: 3x14 turns
L1: 100uH / 15 turns
L2: 3.18uH / 27 turns
L3: 680nH / 11 turns (20MHz trap)
L4: 5uH / 35 turns (5MHz trap).

Input Level	Residual Phase Noise					
P-in	1Hz	10Hz	100Hz	1kHz	10kHz	100kHz
dBm	dBc/Hz	dBc/Hz	dBc/Hz	dBc/Hz	dBc/Hz	dBc/Hz
17,1	-140,0	-152,0	-161,0	-170,0	-172,0	-173,0
16,2	-140,0	-152,0	-160,0	-169,0	-172,5	-173,0
15,3	-140,0	-151,0	-160,0	-169,0	-172,0	-172,5
14,3	-140,0	-151,0	-160,0	-168,5	-171,0	-171,0
13,3	-140,0	-150,0	-160,0	-168,0	-170,0	-170,0
12,3	-140,0	-150,0	-159,0	-168,0	-169,0	-169,0
11,3	-140,0	-149,5	-158,0	-167,0	-168,0	-168,0
10,3	-140,0	-149,0	-158,0	-166,0	-167,0	-167,0
9,3	-138,0	-148,0	-155,5	-164,5	-166,0	-166,0

Residual Phase noise



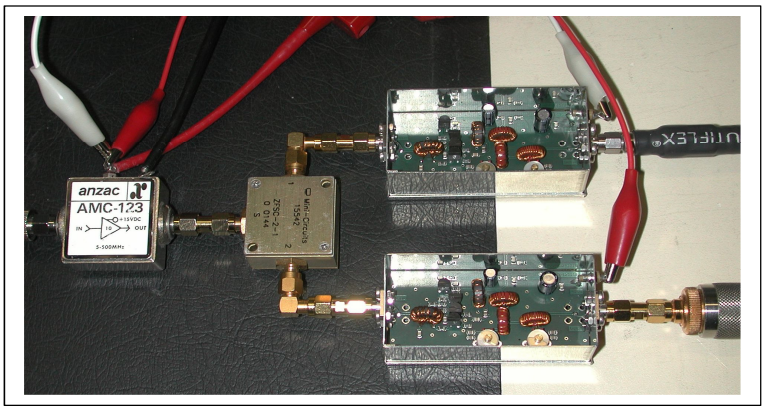
P-in +12.3 dBm Phase noise



P-in +16.6 dBm Phase noise

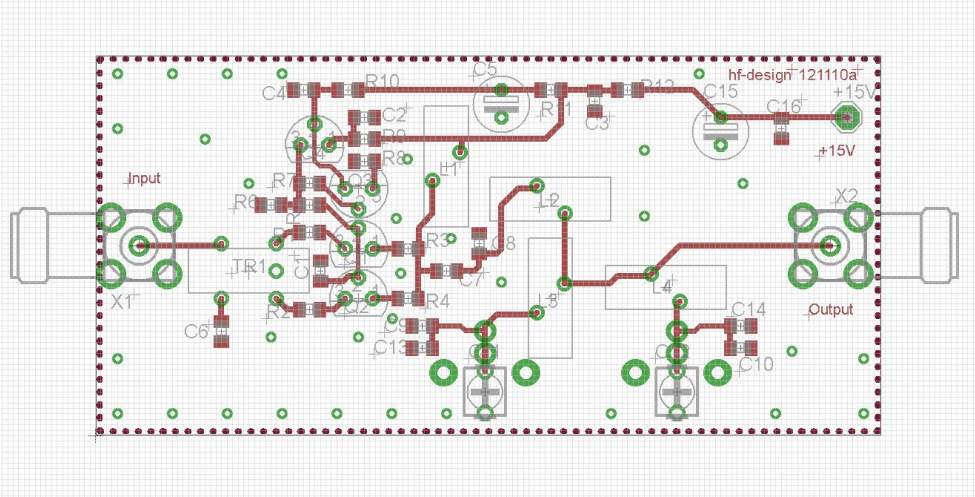
5Mhz P-in dBm	10MHz P-out dBm	Gain dB
20.8	20.9	0.1
20.2	20.9	0.7
19.3	20.6	1.3
18.3	20.0	1.7
17.3	19.0	1.7
16.3	18.0	1.7
15.3	17.0	1.7
14.4	15.9	1.5
13.4	14.8	1.4
12.3	13.6	1.3
11.3	12.4	1.1
10.3	11.3	1.0
9.3	10.2	0.9
8.2	8.9	0.7
7.2	7.7	0.5
6.3	6.4	0.1
5.3	5.0	-0.3

Level response

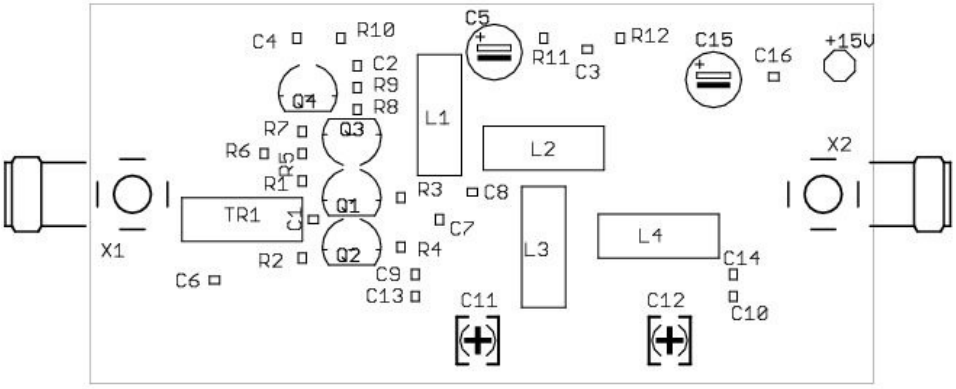


Residual phase noise test setup

The gain response shows an optimum input level range of +13 to +17dBm. The usable range is about +10 to +19dBm.
Variable capacitor C11 is adjusted to notch the 20 MHz harmonic and C12 to notch the 5 MHz fundamental.A PCB was designed to improve the physical and electrical stability. It is a mixed SMD and through holes (THT) design.



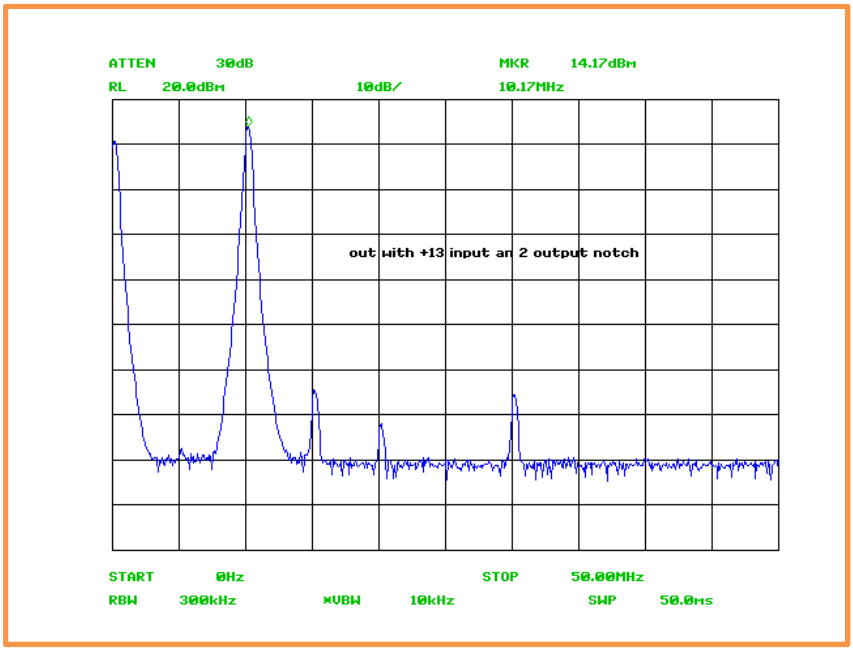
PCB layout



Component locations

Part list

Part	Value	Package	Position X	Position Y	Orientation
			mm	mm	
C1	100n	0805	20,50	15,00	R270
C2	100n	0805	24,50	29,00	R180
C3	100n	0805	45,50	30,50	R90
C4	100n	0805	19,00	31,50	R180
C5	47u/25V	ES-2,5L	37,00	31,50	R270
C6	10n	0805	11,50	9,50	R90
C7	10n	0805	32,00	15,00	R180
C8	82p	0805	35,00	17,50	R270
C9	56p	0805	29,80	10,00	R0
C10	180p	0805	58,80	8,00	R180
C11	30p	3008	35,50	4,00	R270
C12	30p	3008	53,00	4,00	R270
C13	6p8	0805	29,80	8,00	R0
C14	15p	0805	58,80	10,00	R180
C15	100u/25V	ES-2,5L	57,00	29,00	R270
C16	100n	0805	62,50	28,00	R90
L1	100uH	IND_T37	32,00	24,50	R90
L2	3,18uH	IND_T37	41,50	21,50	R0
L3	680nH	IND_T37	41,50	12,50	R90
L4	5uH	IND_T37	52,00	13,50	R180
Q1	2N3904	TO92	24,00	17,00	R0
Q2	2N3904	TO92	24,00	12,50	R0
Q3	2N3904	TO92	24,00	22,50	R180
Q4	2N3904	TO92	20,00	26,50	R0
R1	47R	0805	19,50	18,50	R0
R2	47R	0805	19,50	11,50	R0
R3	10R	0805	28,50	17,00	R0
R4	10R	0805	28,50	12,50	R0
R5	100R	0805	19,50	21,00	R180
R6	1k	0805	16,00	21,00	R0
R7	220R	0805	19,50	23,00	R0
R8	47R	0805	24,50	25,00	R0
R9	1k	0805	24,50	27,00	R0
R10	3k3	0805	23,00	31,50	R0
R11	3k3	0805	41,50	31,50	R0
R12	33R	0805	48,50	31,50	R0
TR1	TRF_T37	TRAFO_T37	14,00	15,00	R0
X1	BU-SMA-H	BU-SMA-H	4,00	17,30	R180
X2	BU-SMA-H	BU-SMA-H	67,00	17,30	R0



Output spectrum response harmonics and sub-harmonic more than 50dBc

The project team is composed by:

-Bruce Griffiths	New Zealand	Principal designer
-Adrian Socnik	Germany	PCB design and testing / characterization
-Luciano Paramithiotti	Italy	Filter design and testing

Reference 1) Low Phase Noise Design: Frequency Multipliers, Bruce Griffiths http://www.ko4bb.com/~bruce/FrequencyMultipliers.html